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DEVELOPMENT OF INSTRUMENTATION TO MONITOR THE RADIAL DEFORMATION OF THE MEDIUM AROUND AN UNDERGROUND OPENING. PART I. SELF-CONTAINED SYSTEM

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Development of Instrumentation to Monitor the Radial Deformation of the Medium Around an Underground Opening

Part I: Self-Contained System

Final Technical Report
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SEPTEMBER 29, 1972 - NOVEMBER 15, 1973

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CONTENTS

LIST OF FIGURES

DEVELOPMENT OF INSTRUMENTATION TO MONITOR RADIAL DEFORMATION
OF THE MEDIUM AROUND AN UNDERGROUND OPENING
FINAL TECHNICAL REPORT - PART I - SELF-CONTAINED SYSTEM
SEPTEMBER 29, 1972 - NOVEMBER 15, 1973

INTRODUCTION

The objectives of this research and development program were to develop two unique types of instrumentation suitable for measuring deflection of the medium surrounding an underground opening. These two instrument systems are referred to as the "Self-Contained System" and the "Laser System."

We are at the end of the second year of a planned 3 year research and development effort. Work performed during the first year is described in the semiannual and annual reports dated August 30, 1971 and March 9, 1972, (No. AD-752072) respectively. Work performed during the first half of the second year is reported in the semiannual report dated September 29, 1972 (No. AD-753274).

This report concentrates on the work performed during the last half of the second contract year and includes a summary of work accomplished followed by detailed technical discussions presented in Part One entitled "Self-Contained System" and Part Two "Laser System."

Work performed under the contract and directed toward self-contained system development resulted in development of two prototypes. The first prototype, which used a punched paper tape recorder to store measurement data, was developed during the first contract year and evaluated in the laboratory and underground during the first part of the second contract year. Because of advancing technology related to programmable, read only solid-state memories, the planned development work was modified about midyear and a self-contained system, using this new technology, was developed during the last half of the contract year. This work is described in detail in Part One of the report.

Work performed under the contract and directed toward Laser System development resulted in design and fabrication of a prototype instrument system and evaluation of the system in the laboratory and at an underground

site near Spokane, Washington. Laser System concept definition was completed during the first contract year and is discussed in the first annual report. Fabrication and evaluation of a prototype was performed during the second year and is covered in Part Two of this report.

The instrumentation developed provides unique tools for the study of stability of underground openings particularly where deformation measurements are required very close to a drilled or blasted opening and where extended periods of automatic data recording are needed.

SUMMARY

During the first contract year, we completed concept selection, component evaluation, and prototype design and fabrication for the Self-Contained System (referred to as Prototype I throughout this report). During the current contract year we have completed laboratory and field evaluation (underground) of the first prototype Self-Contained System and development and preliminary evaluation of the second prototype Self-Contained System (Prototype II). The following summarizes the work described in Part One of this report--Self-Contained System. Summary of the Laser System work is contained in Part Two.

Prototype I used a miniature punched paper tape recorder to store data. During the first half of this contract year we completed laboratory and underground evaluation of Prototype I. This evaluation work is discussed in detail in the semiannual technical report dated September 29, 1972. During initial concept selection for Prototype I we considered using solid-state memory devices for data storage, although conventional solid-state memory devices are volatile and would lose data if the power were interrupted (as might happen if the instrument were exposed to the blast-induced vibration). Read-only memory devices were a possible alternative, but our investigation revealed that the devices then available were not reliable enough for our application.

Since the technology of solid state devices is advancing rapidly, Programmable Read Only Memory (PROM) devices were available by late 1972 that would meet the requirements of the Self-Contained System. Since this type of memory has the probability of being less costly and more reliable than the mechanical recording device, the second prototype instrument was built using PROM's for data storage. This modification to the planned work is covered by Amendment 6 to the contract.

As a result of this changed work scope, Prototype II was built. Very limited laboratory evaluation was completed on Prototype II and no underground evaluation work was performed. Prototype II does have several advantages (listed below) over Prototype I and appears to be a better overall self-contained system instrument.

- Smaller physical size (shorter)
- Longer operating life
- Larger data storage capacity
- More reliability (although this has not been determined in underground evaluation)
- More rugged construction (no moving parts)
- Comparable cost.

DISCUSSION

A thorough description of the Self-Contained System operating goals and characteristics was included in previous reports, however an abbreviated version is included here for convenience. The Self-Contained System should:

- measure radial deformation of the rock around an underground opening,
- be self-contained and operate unattended for 1 week or more; in other words, retrieve and retain deformation data without external connections or wire protruding into the excavation,
- fit into a small bore hole (2 in. as a goal),
- survive the environment including humidity, temperature, shock and vibration,
- have a resolution and accuracy of ±0.005 in.,
- have good reliability, and
- be relatively inexpensive.

Prototypes I and II both consist of:

- an LVDT (linear variable differential transformer) to convert linear mechanical motion to an electrical signal,
- a data recording device (mechanical in Prototype I and electronic in Prototype II),
- electronics to process the electrical signal from the transducer and to provide logical operation and control,
- batteries to power the electronics, transducers, and data recording device,
- a containment assembly to hold and protect components, and
- an anchoring system to position the instrument such that relative movement between the front and back of the bore hole would result in similar movement in the LVDT. Another function of the anchoring system was to provide a considerable amount of protection for the instrument from shock and vibration (primarily by isolation).

Original plans for the Self-Contained System development included fabrication of two additional prototypes (Prototype I) and assembly of the externally powered and recorded systems to replace the self-contained prototypes during extended operating periods. This work was planned for the second half of the current contract year.

When the state-of-the-art of PROM's advanced to the point where they were suitable for use in the self-contained system, it was decided to replace the punched paper tape recording systems with a second prototype self-contained system using PROM's as a data recording device. In the remainder of the report this second prototype is referred to as Prototype II to distinguish it from Prototype I, the original prototype which used a mechanical data recorder.

The following describes development of Prototype II in two sections: Development of the Electronics, and Packaging and Laboratory Evaluation of Prototype II.

ELECTRONICS DEVELOPMENT

The primary objective of this effort was to develop the electronics package for a self-contained instrument suitable for measuring deformation of the medium surrounding an underground opening. This effort included two prototypes, each of which is capable of achieving the objective. Prototype I provided the drive circuitry to operate a punched paper tape recording unit; documentation of Prototype I development is contained in the first annual report. Prototype II includes the drive circuitry and read/write logic for a self contained non-volatile solid state memory integrated circuit (IC) for 256 word x 8 bit data storage, expandable to 1024 word x 8 bit data storage.

Prototype I was developed, fabricated and laboratory and field tested prior to the Semiannual Technical Report (September 29, 1972). A desire to further reduce power requirements, reduce instrument length, increase recording capacity, and improve overall reliability led to the development of Prototype II with solid state memory. Preliminary laboratory testing was begun with Prototype II installed in its containment tube. An INTEL C1702A memory reader was developed and fabricated to facilitate reading the stored data. The reader was tested and used (by connection

to an ASR-35 off-line teletype) for monitoring stored data while Prototype II was being evaluated. Prototype II design greatly reduced power requirements. The operating capabilities of Prototype II were also improved over those of Prototype I to permit more effective operation under the anticipated adverse operating conditions. Some of these improvements include:

- shorter overall length
- longer operating life
- longer shelf life after final assembly
- larger data storage capacity
- more reliability (although this was not established in underground tests)
- more rugged construction (no moving parts)
- no more costly
- less preventive maintenance.

The following includes the circuit description, operating procedure, and schematic diagrams for Prototype II and the INTEL C1702A memory reader (developed to facilitate reading the stored data).

INSTRUMENT CIRCUIT DESCRIPTION

Definitions

- STANDBY MODE - Connecting the power pack to the electronics automatically initiates the STANDBY MODE; no power is supplied to the logic.
- QUIESCENT STATE - A minimal amount of CMOS logic is powered in the QUIESCENT STATE to permit acceptance of further commands (both internal automatic and external manual commands).
- AUTO MODE - The AUTO MODE permits the unit to make automatic A/D conversions and subsequent data storage at the rate selected by the rate selector switch.
- READOUT COMMAND - A READOUT command initiates an A/D conversion and a serial readout on the LED's, Most Significant Bit (MSB) first. The information is 10-bit binary where illuminated green LED's represents a 1 bit and illuminated red LED's represents an Ø bit; LED's flash at approximately 1 Hz intervals.

- POSITION CALIBRATION COMMAND - POSITION CALIBRATION command illuminates a set of LED's to permit LVDT reference calibration. Red LED's indicate outside of reference and green LED's indicate inside of reference. An automatic timeout (approximately 60 sec) terminates the command.
- MANUAL MODE - The MANUAL MODE is the only mode permitting LVDT reference calibration. Commanding the unit into the QUIESCENT STATE will automatically place the unit in the MANUAL MODE of operation.

Operator

External commands to the self-contained system electronics are accomplished via a light beam from a regular flashlight or miner's headlamp. Information is output to the operator via dual redundant red and green LED (light emitting diode) displays. See Figure 1 for the self-contained system block diagram and Figure 2 for detailed information on control logic sequence.

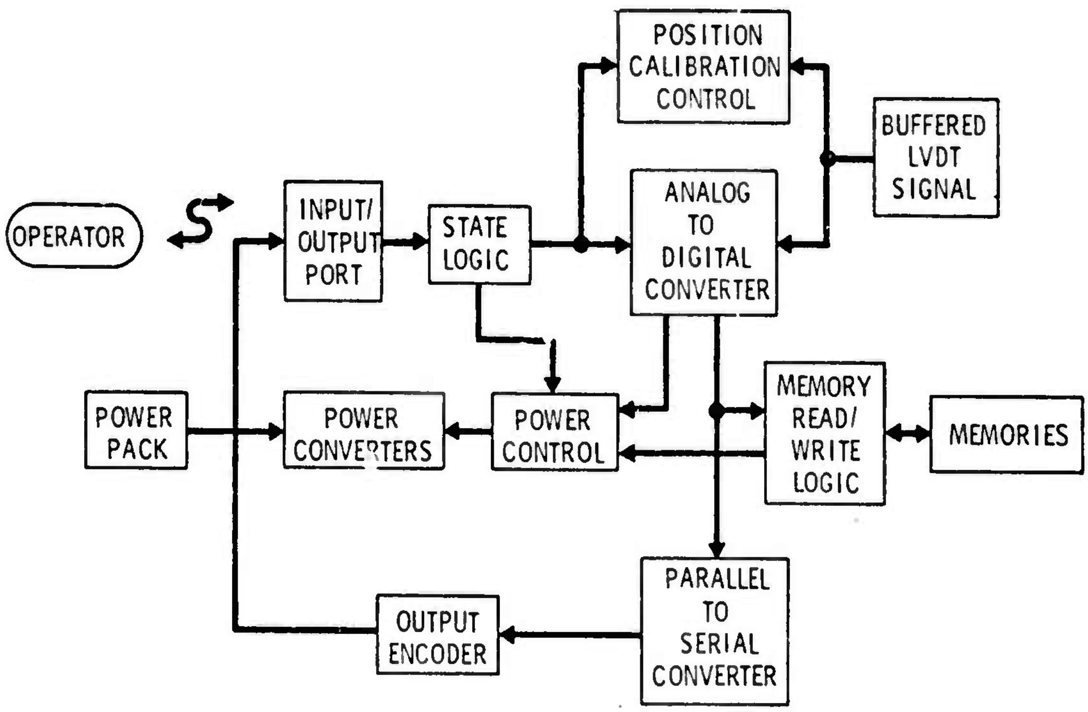


FIGURE 1. Prototype II with Solid State Memory Self-Contained System Block Diagram

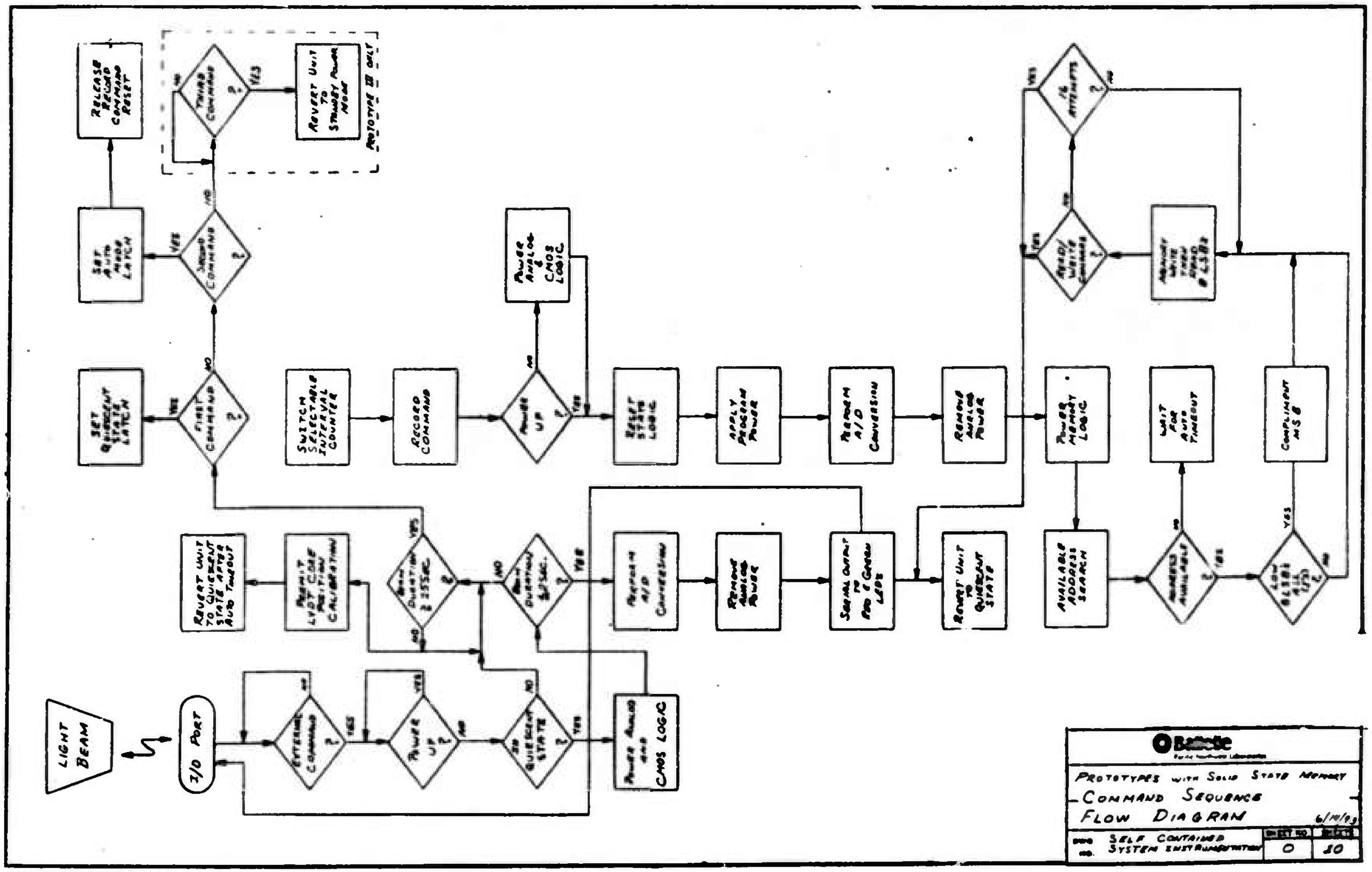


FIGURE 2. Command Sequence Flow Diagram

Input/Output Port

Light input is sensed by two redundant photo transistors and buffered by an emitter follower to the state logic; light interval and sequence determines interpretation. Operator information from the output encoder is displayed through red and green LED's for operator interpretation.

Steady red or green lights inform the operator of the relative position of the LVDT (linear variable differential transformer) core with respect to a predetermined reference point:

- green indicates inside of reference
- red indicates outside of reference
- flashing red and/or green lights indicate ADC (analog to digital converter) output, most significant bit first
- green indicates a binary 1 bit, and
- red indicates a binary Ø bit.

State Logic

State is the condition or "state" of the electronic circuitry (some off and some on) needed to perform a function. A specific state is needed to perform a specific function. State logic controls the operation and sequence of operation of the instrument which insures that operations and commands are carried out in an orderly fashion. It also determines the priority of requests and commands the power control circuitry. States can be incremented by the internal clock only.

The state logic steps sequentially through four states (Ø-3). Power to the state logic is applied externally by an operator request or internally by the time-interval counter if in the AUTO MODE. The functions accomplished in the various states are as follows:

State Ø: RESET commands are issued to prepare the instrument for command interpretation. The POWER CONTROL is then informed to apply ±15 V of power to the analog signal devices such as LVDT, ADC (analog to digital converter), and bipolar reference source.

State 1: If the state is externally caused the absence of a light beam at any time during this state is interpreted as a READOUT command. A continuous presence of light during this state is interpreted as a POSITION CALIBRATION command unless in the AUTO MODE, in which case a READOUT command is initiated. On the other hand, if the state is internally caused, program power is applied to charge the memory program storage capacitor through a current limiting constant current source. An ADC CONVERT command is then issued.

State 2: State 2 initiates a RECORD command if the state logic was sequenced to this state by the time interval counter; otherwise, no command is issued. A RECORD command informs the POWER CONTROL logic to apply memory logic and drive power.

State 3: This is the waiting state. Upon completion of a parallel-to-serial readout, memory read/write cycle, or auto time-out, a POWER DOWN command is issued to remove power no longer required. The unit reverts back to the QUIESCENT STATE. Should the internal time interval counter request a convert/record cycle while in that state, any external command (not an overriding command) is immediately aborted and the state logic is reset to State Ø in order to initiate a new "power up" cycle.

Position Calibration Control

Upon command from the state logic, the LVDT signal conditioner output voltage is compared with an internal reference voltage to permit position calibration during instrument installation.

Analog to Digital Converter (ADC)

The ADC receives its power from ±15 V regulated DC-DC converters turned on during State Ø. Upon command from the state logic, a 10-bit binary A/D conversion is made with a tracking type ADC. The binary data are available at the input to the parallel-to-serial converter, while only the eight least significant bits are available to the memory. Upon completion of an A/D conversion, an end-of-convert (EOC) signal is issued to indicate that information to state logic and to inform Power Control to remove the ±15-V regulated power to the analog circuitry.

Power Pack

The power pack consists of one 5.4-V mercury battery (non-rechargeable) to power the quiescent powered CMOS (Complimentary symmetry metallic oxide semiconductor) logic and six 2-V GATES lead-acid batteries to provide 6 and 12 V to the remaining circuitry.

Power Converters

DC-DC voltage converters are used, as required, to minimize the size of the power pack and to provide power in the proper form for operating the analog circuitry and memory read/write drivers. The 6-V source provides power to the regulated ±15-V converters, while the 12-V source provides power to the +60-, +75-, and -10-V converters required for the memory storage units (PROM's) INTEL C1702A.

Power Control

The power control logic consists of current switches to control power to the various circuits in the unit as necessary. Power is applied only when and where essential to the proper operation of the instrument. Input is controlled by the state logic, A/D converter, and memory read/write logic.

Parallel-to-Serial Converter

In response to an operator readout command, an A/D conversion is made of the LVDT signal conditioner output. The 10-bit ADC output is converted to serial form by a parallel-to-serial shift register and sent to the output encoder, most significant bits (MSB) first. A binary bit is converted each second, taking a total of 10 sec to display each of the bits in succession.

Output Encoder

The output encoder converts electrical information into red and green displays for operator interpretation; two of each are used for redundancy. The encoder receives its inputs from the position-calibration-control-logic and parallel-to-serial converter.

Memory Read/Write Logic

The memory read/write logic controls the handling of binary data recorded in the nonvolatile reprogrammable memories. The several functions performed by this subsystem are as follows:

- The address register sequentially scans the memory, and the contents of each address are read until the first address where no data have been previously stored is located. This address will be the next address for data storage.
- Only the least significant eight bits from the 10-bit ADC are recorded. If these eight bits should appear identical to an unwritten word, the MSB is complemented to permit recording at least one bit at each memory address. Otherwise, a written address could appear as an unwritten one, thus losing a data word.
- A write cycle follows the recognition of an unwritten address, ADC end-of-convert (EOC) signal and State 3. The write cycle includes address complementing, application of high voltages and power required for the write cycle, and a program pulse to accurately control the total energy supplied to the memory.
- A read cycle follows to compare the written data with the ADC output to verify accuracy of memory contents. If the written data disagrees with the ADC output, a second write/read cycle occurs. A maximum of 16 cycles is permitted before automatic power down.

INSTRUMENT OPERATION AND OPERATING CHARACTERISTICS

Unit Preparation

WARNING: Insertion or removal of INTEL C1702A memories should be performed with the battery pack disconnected. Observe proper direction of insertion. Dot on memory must be in same corner as notch on memory connector. Use an IC extraction tool to guard against accidental lead damage during removal.

1. Install six freshly charged and properly functioning Gates "D" cells and one fresh 5.4-V mercury cell into the battery holder, observing polarity.

2. Insert from one to four erased INTEL C1702A 256 x 8 bit memories into the memory sockets starting with the one closest to the battery pack, observing polarity. The memory can be erased with high intensity, short wave ultraviolet light, e.g., 3/4 in. from the lamp of an Ultra-Violet Products, Inc., Model S52 for 15 min. Reading the memory on the PROM C1702A Reader connected to an ASR/KSR-33 or -35 teletype will provide a check to insure a cleared (erased) memory.

3. Depress the desired recording rate switch to ON; all others should be OFF. Positions 1-4 offer rates of 31, 1000, 2000, and 4000 sec, respectively.

4. Connect the battery pack to the electronics package. Keep the ambient light off the end piece to reduce "ambient current" through the photo transistors and to minimize standby power requirements prior to placing unit into operation.

External Commands

1. The first 25- to 30-sec duration light beam directed at the photo transistors causes the electronics to switch from the STANDBY MODE to the QUIESCENT STATE. When a pair of LED's are lit, the light source may be removed and POSITION CALIBRATION initiated. Upon completion of the command, the unit will be in the QUIESCENT STATE.

2. A light beam of approximately 1 sec duration will be accepted as a READOUT command.

3. A light beam of 3 sec or longer, while in the MANUAL MODE, will be interpreted as a POSITION CALIBRATION command. In the AUTO MODE, the same command would be interpreted as a READOUT command. (A POSITION CALIBRATION command in the AUTO MODE serves no useful purpose.)

4. A second 25- to 30-sec duration light beam will be accepted as an AUTO MODE command. The light source should be removed when the LED's turn off. The first data are recorded at initialization of the AUTO MODE command.

Operating Characteristics

1. Resolution
   LVDT - 0.005 in./ADC bit

2. QUIESCENT STATE, AUTO MODE and POWER DOWN commands override other commands.

3. While processing any command, no further READOUT or POSITION CALIBRATION commands will be accepted.

4. A POWER DOWN command can only be accepted in the AUTO MODE. The operator can be assured that POWER DOWN command will be accepted if the LED's continue to flash while the command is in progress and if they stop flashing at the termination of command recognition. A POWER DOWN command (or reversion to STANDBY MODE) is essential immediately following completion of data collection. This action insures power removal to all digital logic prior to power failure due to battery drain.

5. The unit retains the operating mode and the selected state, even during momentary power loss.

6. Prototype II can only be reverted to the STANDBY MODE by disconnecting the power pack for a minimum of 5 sec.

7. More than adequate power is available to record 1024 A/D conversions over a 3-week period if factory fresh and freshly charged batteries are used where required. Table 1 compares the anticipated power available to write and fill one to four PROM's at various recording rates. This table was prepared from preliminary information available from Prototype II and assumes that the instrument will not be powered up for more than 10 min for POSITION CALIBRATION and READOUT commands combined.

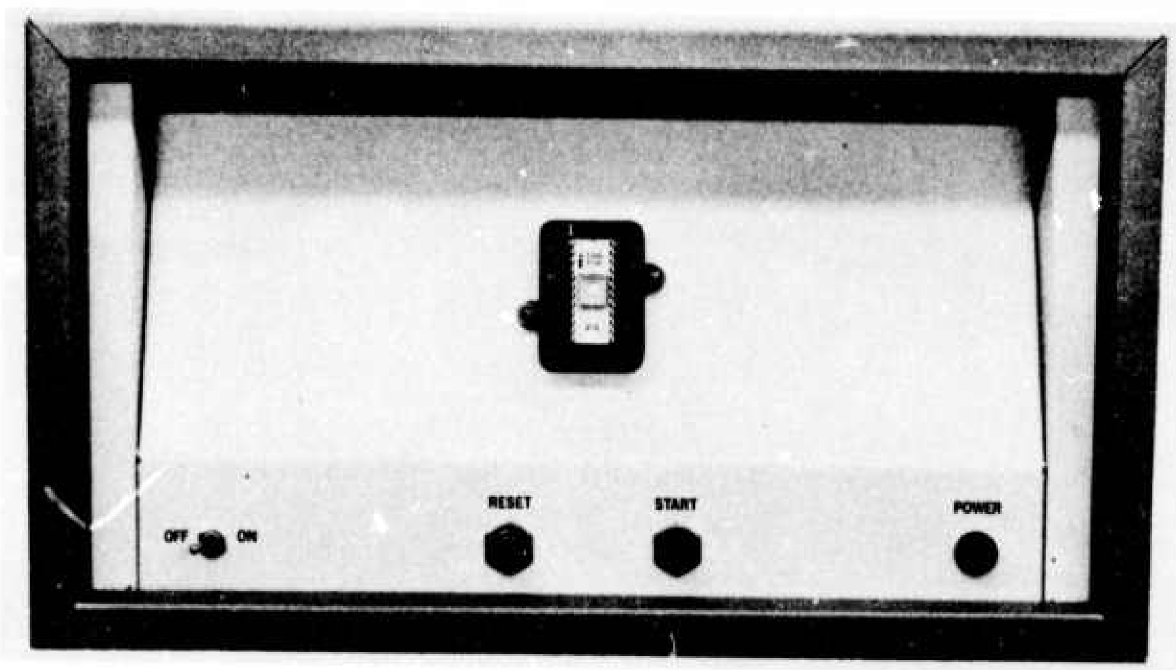
   The actual power available is greater at laboratory temperatures. Battery power available, however, must meet manufacturer's specifications at the time of installation.

TABLE 1. Anticipated Power Available

Mode of Operation			Units	Maximum Number of Records	Record Interval (seconds)
STANDBY	MANUAL	AUTO			
4	2	22	days	1024	2000
12	5	11	days	1024	1000
300	50	9	hours	1024	33.3
10	4	16	days	768	2000
5	3	22	days	512	4000
12	7	11	days	256	4000
20	7	3	days	256	1000

PROM READER CIRCUIT DESCRIPTION

The memory reader permits printing the data recorded by the self-contained instrument via teletype, one memory at a time. An ASR 33/35 or KSR 33/35 teletype set for a 20 mA current loop may be used; see Figure 3, for the PROM Reader Block Diagram. This system is designed to retrieve information from an INTEL C1702A integrated circuit.



INTEL PROM READER

Information stored in the memories is in binary form. The reader converts the binary information to binary-coded-decimal (BCD). The BCD is converted to ASCII and output through a Western Digital TR1402A transmitter

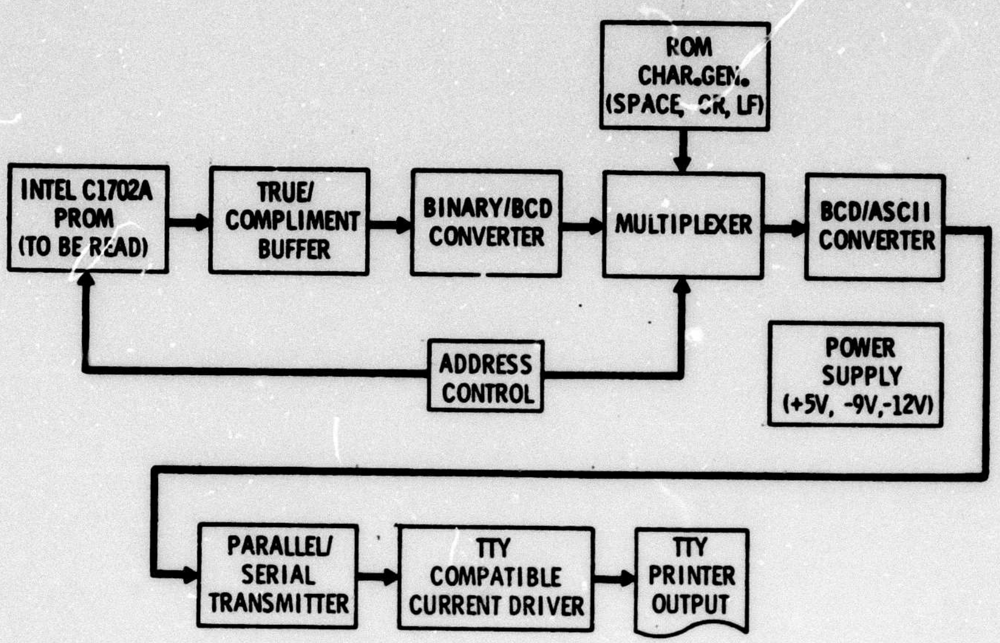


FIGURE 3. INTEL PROM Reader Block Diagram

206	236	236	226	206	112	112	112	111	112	111	112	111	111	112	112	111	111
234	234	235	235	235	235	235	235	236	242	241	242	241	242	242	241	242	241
241	241	242	241	242	112	113	112	112	113	110	113	112	110	112	111	112	112
144	144	144	144	144	143	143	143	143	143	144	143	144	143	144	144	144	144
143	144	143	144	143	144	143	143	144	144	144	144	144	144	227	228	227	227
227	227	228	228	228	238	228	208	238	213	228	222	222	228	229	228	228	228
239	232	238	213	232	232	212	239	320	222	222	221	221	220	222	222	148	148
148	149	149	149	149	149	149	150	150	150	151	150	153	152	153	152	152	152
151	152	152	151	153	152	152	153	153	154	222	223	222	223	222	223	223	223
222	222	272	242	202	202	203	222	213	242	222	222	222	224	223	203	223	234
223	233	223	233	233	223	243	243	233	233	224	234	203	224	223	204	224	204
205	233	234	234	234	234	243	283	234	283	234	224	283	283	283	224	225	285
234	234	244	235	234	284	234	234	234	224	234	234	224	234	224	224	204	204
233	234	234	234	234	234	224	234	283	284	233	223	204	284	233	204	223	204
234	243	244	234														
226	224	223	234	204	203	224	223	223	223	224	224	234	234	234	224	224	243
273	323	338	322	323	372	232	333	384	233	223	332	338	223	333	333	382	223
332	323	234	233	338	333	233	322	232	323	238	223	222	233	333	232	330	332
233	323	348	232	232	234	333	333	232	323	328	232	232	223	303	322	333	323
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323	222	233	333	333	333	232	232	322	333	332	228	322	222	223	322	332	322
333	333	233	333	233	322	222	323	223	322	232	323	302	333	233	323	322	332
332	333	233	232	332	232	333	333	332	233	333	232	322	332	232	320	320	223
332	232	323	323														

FIGURE 4. Teletype Printout

for teletype compatible input. The reader prints an address containing all 1 bits or all Ø bits which correspond to red or green LED displays as zero. Since only the eight LSB's are recorded in memory, the largest number which can be printed is 256, corresponding to octal 377. Figure 4 illustrates a sample teletype printout from one filled and one partially filled PROM.

An internally programmed read-only memory, Signetics 8223, provides spaces to separate the data words and carriage return/line feeds to separate the lines; 18 address contents are printed per line.

PROM Reader Operation

The recommended operating procedure is as follows:

1. Insert the memory to be read in the reader and be certain that the dot on memory is aligned with the 1 on the mating reader socket. Note that no leads have been bent under during insertion.

2. Turn on the C1702A Reader.

3. Select TTY (teletype) on-line.

4. Depress Reset Switch and then Start Switch on the reader. Printing operation may be halted at any time by depressing Reset.

5. Reverse the above procedure to turn off.

Teletype Interface

The ASR/KSR-33 or ASR/KSR-35 Teletype to be connected to the PROM Reader must be wired for a 20 mA neutral signal if not already wired for it. If needed, the modification for an ASR/KSR-33 can be accomplished as follows:

1. Remove the cover of the Teletype.

2. Move the purple wire from Terminal 8 to Terminal 9 of Terminal Strip 151411 located at the lower left of the Teletype as viewed from rear.

3. Move the white-blue wire from Terminal 4 to Terminal 5 of the same terminal strip.

4. Move the brown-yellow wire from Terminal 3 to Terminal 5 of the same terminal strip.

5. Move the blue wire from Terminal 3 to Terminal 4 or Power Resistor 181816. This resistor is located at the center of the right side of the Teletype as viewed from the front with the cover removed. When the cover is in place, the resistor can be seen centered under the removable plate on the right side.

Refer to the following Table 2 for connections between the Reader and Teletype.

TABLE 2. Teletype Interface Connections[a]

PROM Reader	ASR/KSR-33	ASR/KSR-35
AN A (RCV+)	P2-8	TS-8
B (RCV-)	P2-7	TS-7
C (Shield)		

(a) Teletype Corporation wiring diagrams 6353 WD (sheet 1) or 7833 WD (sheet 1) are useful in making the changes, but not mandatory.

PACKAGING AND LABORATORY EVALUATION

Upon completion of the electronics development and fabrication for Prototype II, the instrument was packaged and preliminary evaluation conducted. The package used was similar to that used successfully in Prototype I. It consists of a stainless steel shell with an end plug fitted to each end. The end plugs are sealed to the tube with elastomer "O" rings. One end plug has the LVDT body attached to it. The other end has a window through which the phototransistors are activated and the LED's observed and is connected to the shallow anchor mechanism. Anchors and shell assemblies are described in detail in the Semi Annual (September 29, 1972) Report.

All circuit boards, electronic components and batteries were arranged and inserted into the containment shell. The finished layout is shown in Figure 5. The overall length of Prototype II (excluding anchors) is 59 9/16 in., which is about 18 1/2 in. shorter than Prototype I. Figure 6 shows a portion of the circuit boards with four PROM's installed; Prototype II Electrical Schematics are contained in Appendix A.

Two calibration runs were made with the instrument completely assembled; the first run was made in the CALIBRATE MODE. A dial caliper was used to

measure the LVDT core movement. Visual readout was recorded for each 0.250 in. of core movement from 0 to 3 in. of travel. The results of this run are shown in Table 3.

The second calibration run was made in the AUTOMATIC MODE with a recording cycle of 31 sec. The LVDT core was left at each setting for 45 sec to ensure one recording. The PROM was removed from the instrument and read out on the PROM Reader-Teletype combination. This printout is shown in Table 4.

The results of both calibration runs showed the Δ change for a given core change was lower than it should be. The gain of the instrument, which was found low, was adjusted and checked. No other calibration runs or laboratory evaluations were conducted because all available funding had been expended.

Before development of Prototype II can be considered complete, additional laboratory evaluation (including calibration and environmental test) and underground evaluation should be performed. These additional evaluations were not performed under the contract due to limited funding.

During evaluation of Prototype I, we found the instrument had a large temperature-dependent error. Investigation into the cause of this error revealed that almost all the error originated in the LVDT. In discussing the problem with the LVDT vendor, we learned that the large error probably occurred because the LVDT used is a completely new design made specifically for this application. The temperature-induced error in the LVDT which we measured (and which was confirmed by the vendor) is at least 10%/100°F. The vendor can add temperature compensation to the existing LVDT's to correct this error to 3% or better. Since that correction is not enough to eliminate the need for obtaining calibration curves for various temperatures, we decided not to have the temperature compensation modifications made.

Since Prototype II uses the same LVDT as Prototype I it needs to be calibrated at various temperatures to provide data that meet the accuracy goals.

TABLE 3. Visual Readout of Prototype II During Initial Calibration Runs

Dial Caliper Setting, in.	Visual Readout[a]	Decimal Equivalent	Change from Previous Reading	Decimal Equivalent of Eight Least Significant Bits[b]
0	0100000111	263		7
0.250	0100110111	311	48	55
0.500	0101100110	358	47	102
0.750	0110010011	403	45	147
1.000	0111000010	450	47	194
1.250	0111110000	496	46	240
1.500	1000100000	544	48	32
1.750	1001001111	591	47	79
2.000	1001111101	637	46	125
2.250	1010101010	682	45	170
2.500	1011011001	729	47	217
2.750	1100001000	776	47	8
3.000	1100101001	809	33	41
0	0100000110	262		6

(a) 0 was indicated by a red flash while 1 was indicated by a green flash.

(b) Derived from visual readout but should agree with recorded data; see page 17.

TABLE 4. Copy of the Teletype Printout from the PROM Used During Initial Calibration Run of Prototype II

```
007 007 008 056 056 102  140 147 193 195  242 242 034 033 080 080 126 171
171 218 218 009 009 042  069 008 008 008  008 008 000 000 000 000 000 000
```

	Number	
	1	
Line one	2	0.000 in.
	3	
	4	0.250
	5	
	6	0.500
	7	Recorded while moving to next setting
	8	0.750
	9	1.000
	10	
	11	1.250
	12	
	13	1.500
	14	
	15	1.750
	16	
	17	2.000
	18	2.250
Line two	1	
	2	2.500
	3	
	4	2.750
	5	
	6	3.000
	7	Recorded while moving to next setting
	8	
	9	
	10	0.000
	11	
	12	

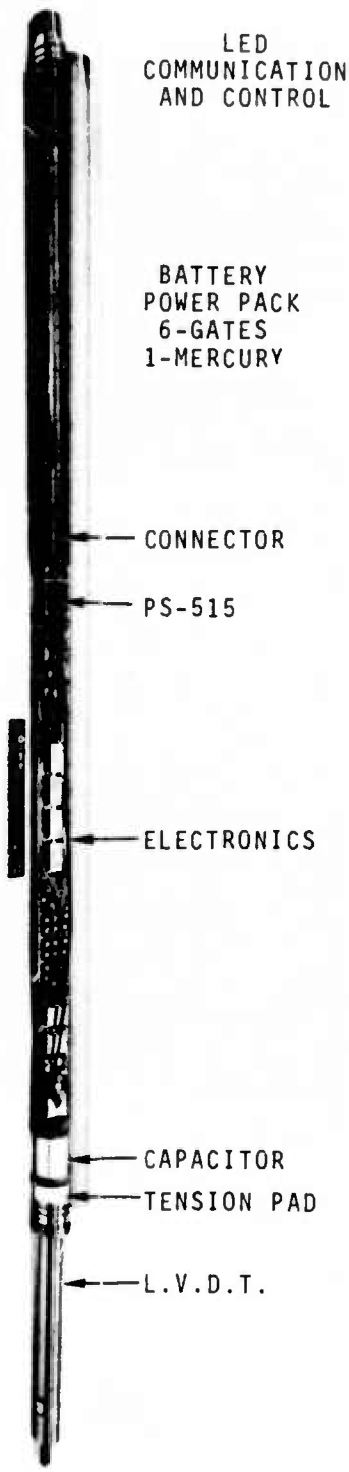


FIGURE 5. Prototype II with Solid State Memory

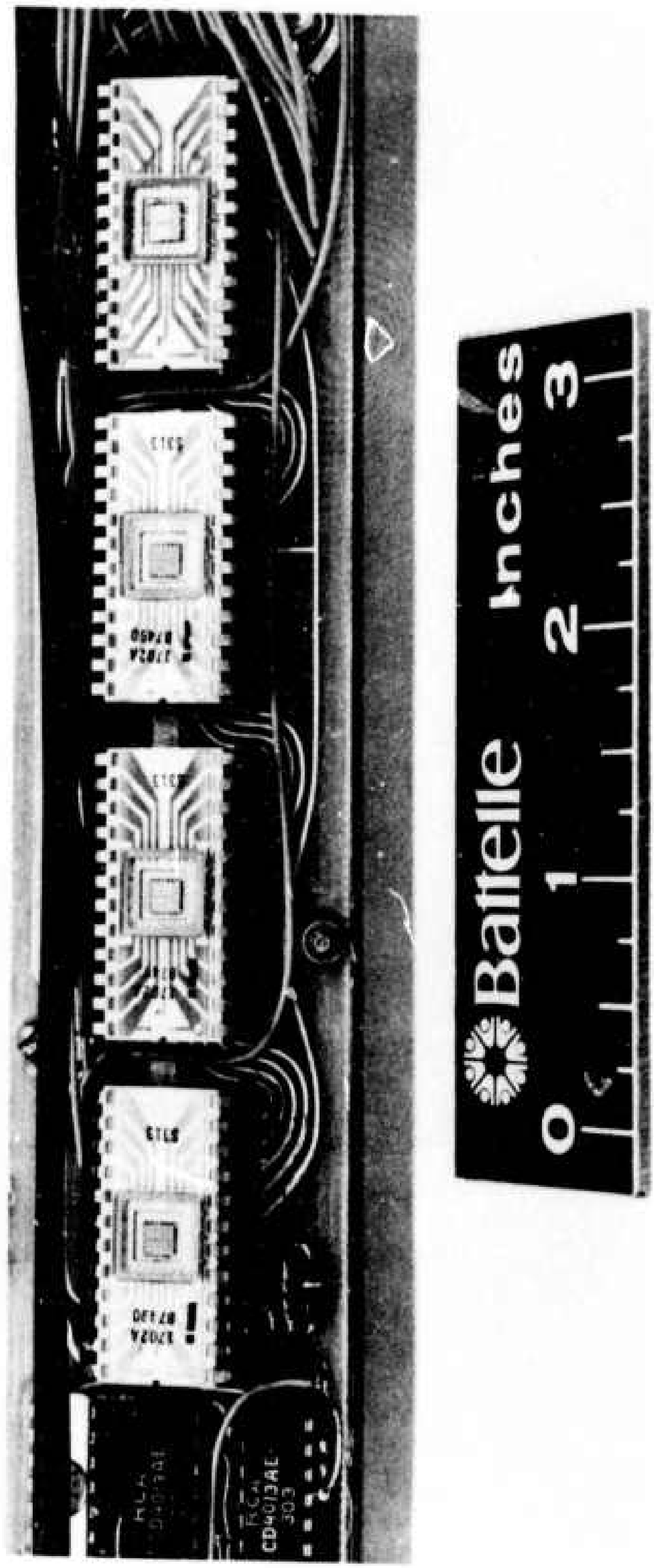


FIGURE 6. PROM's Installed in Prototype II

APPENDIX A

PROTOTYPE II SELF-CONTAINED
SYSTEM ELECTRIC SCHEMATICS

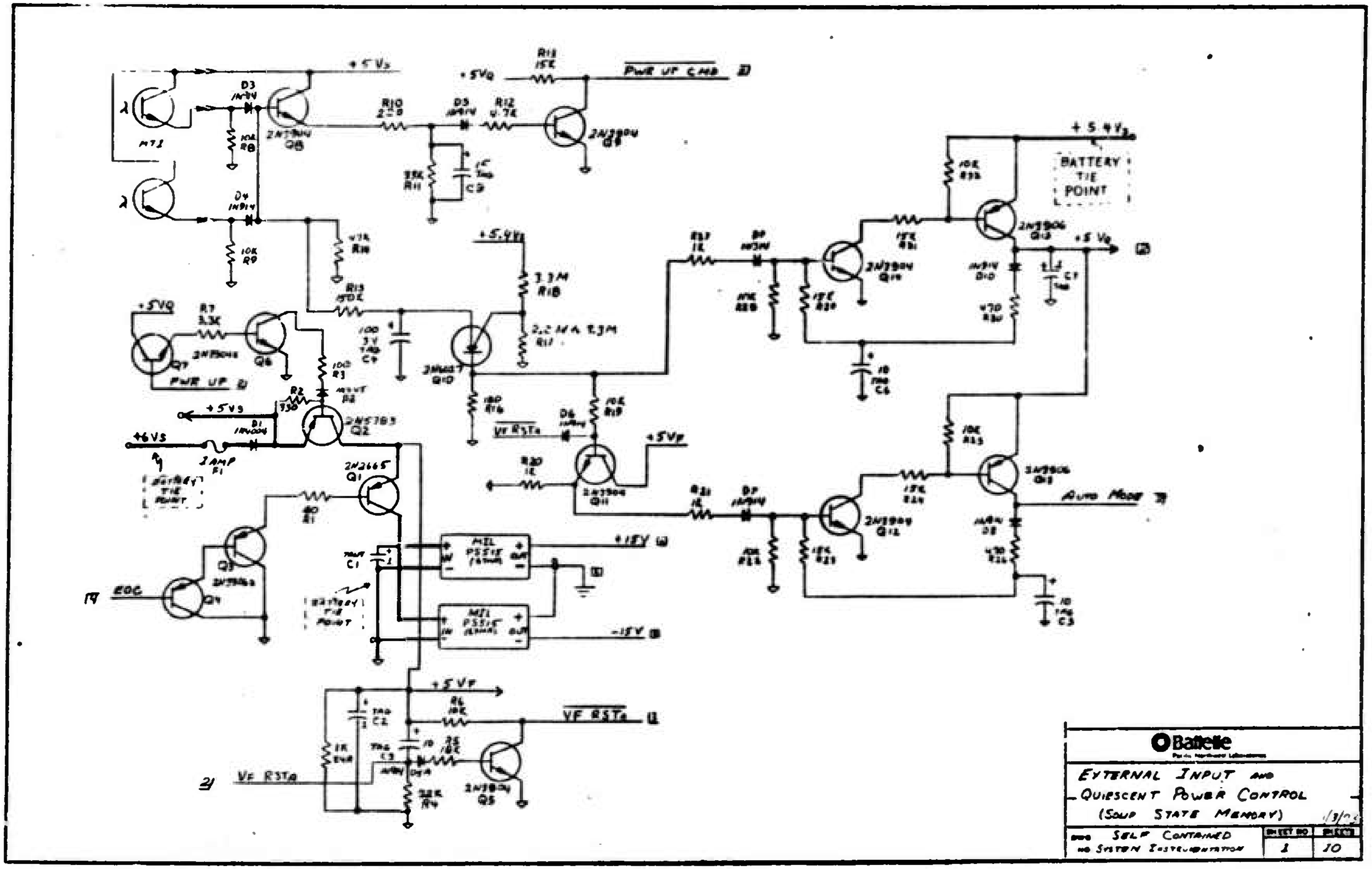


FIGURE A-1. External Input and Quiescent Power Control (Solid State Memory)

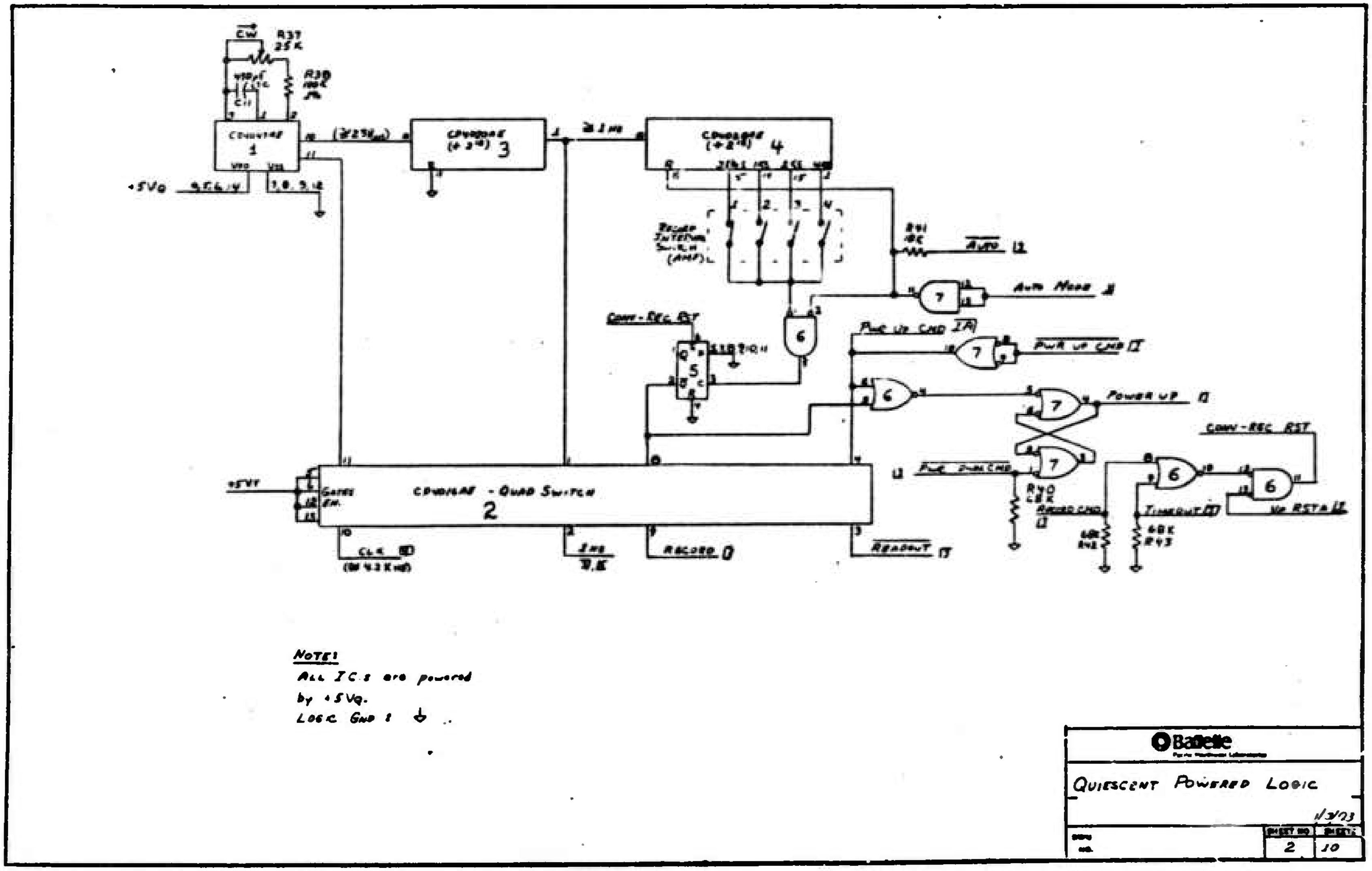


FIGURE A-2. Quiescent Powered Logic

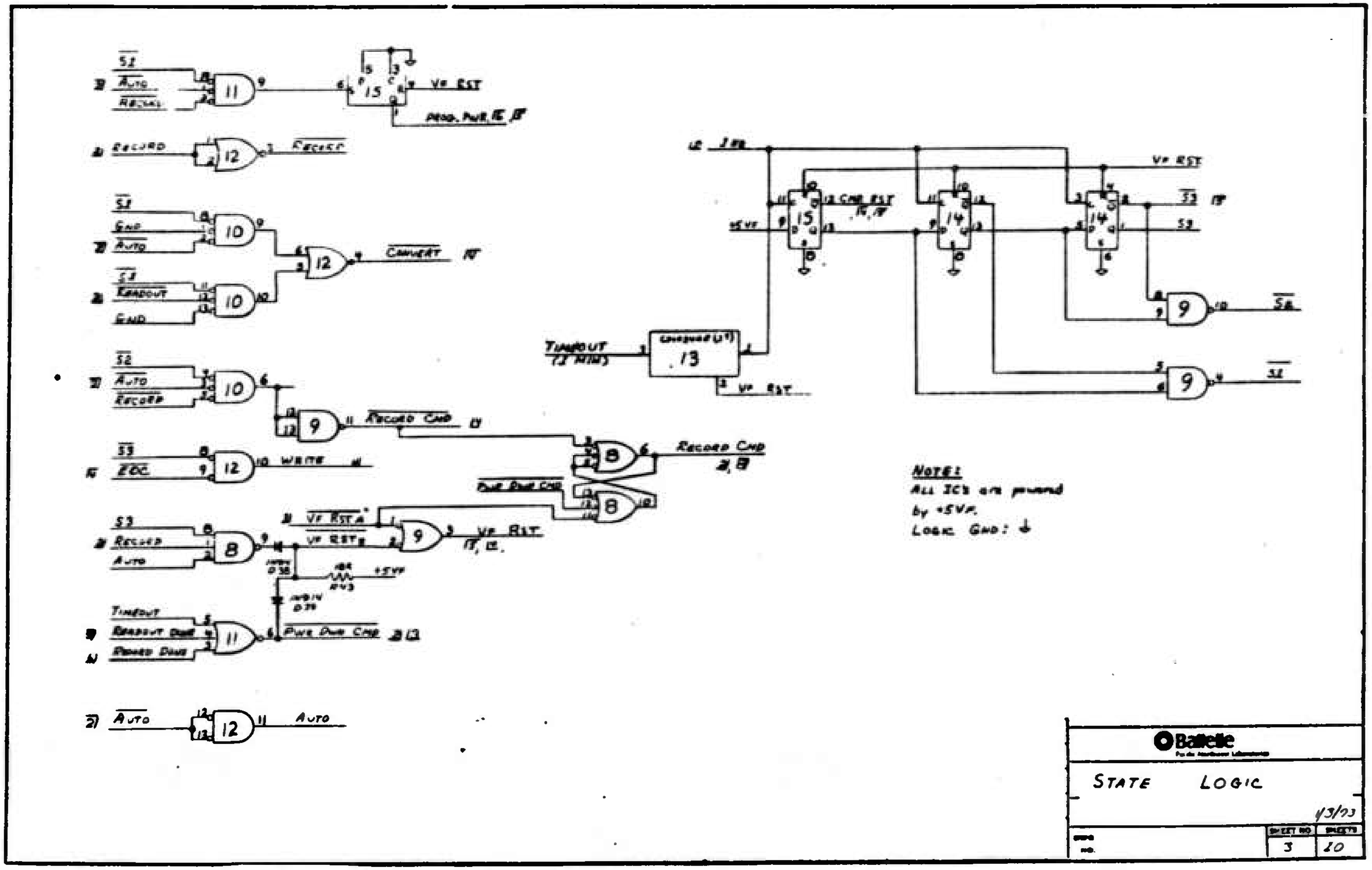


FIGURE A-3. State Logic

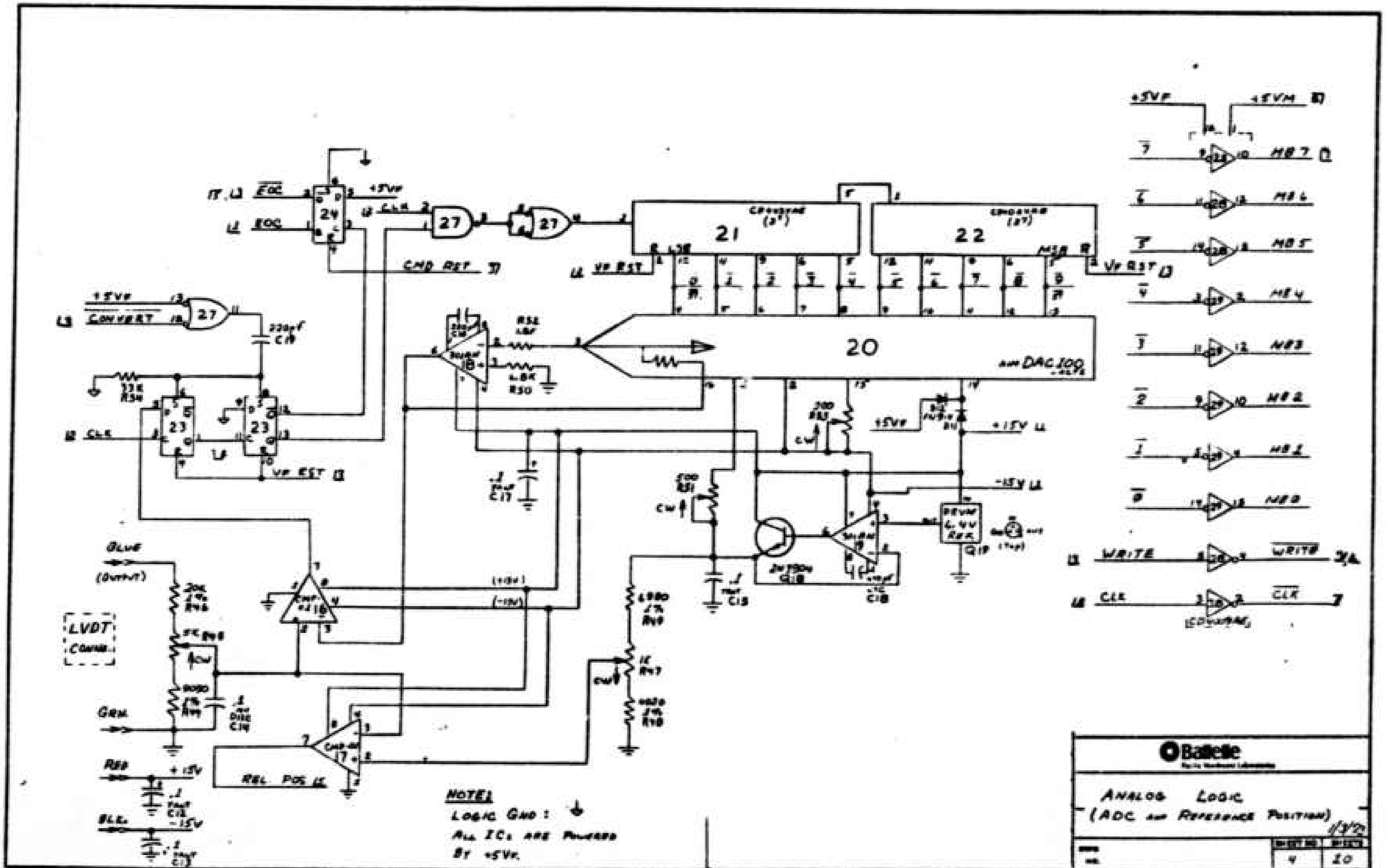


FIGURE A-4. Analog Logic (ADC and Reference Position)

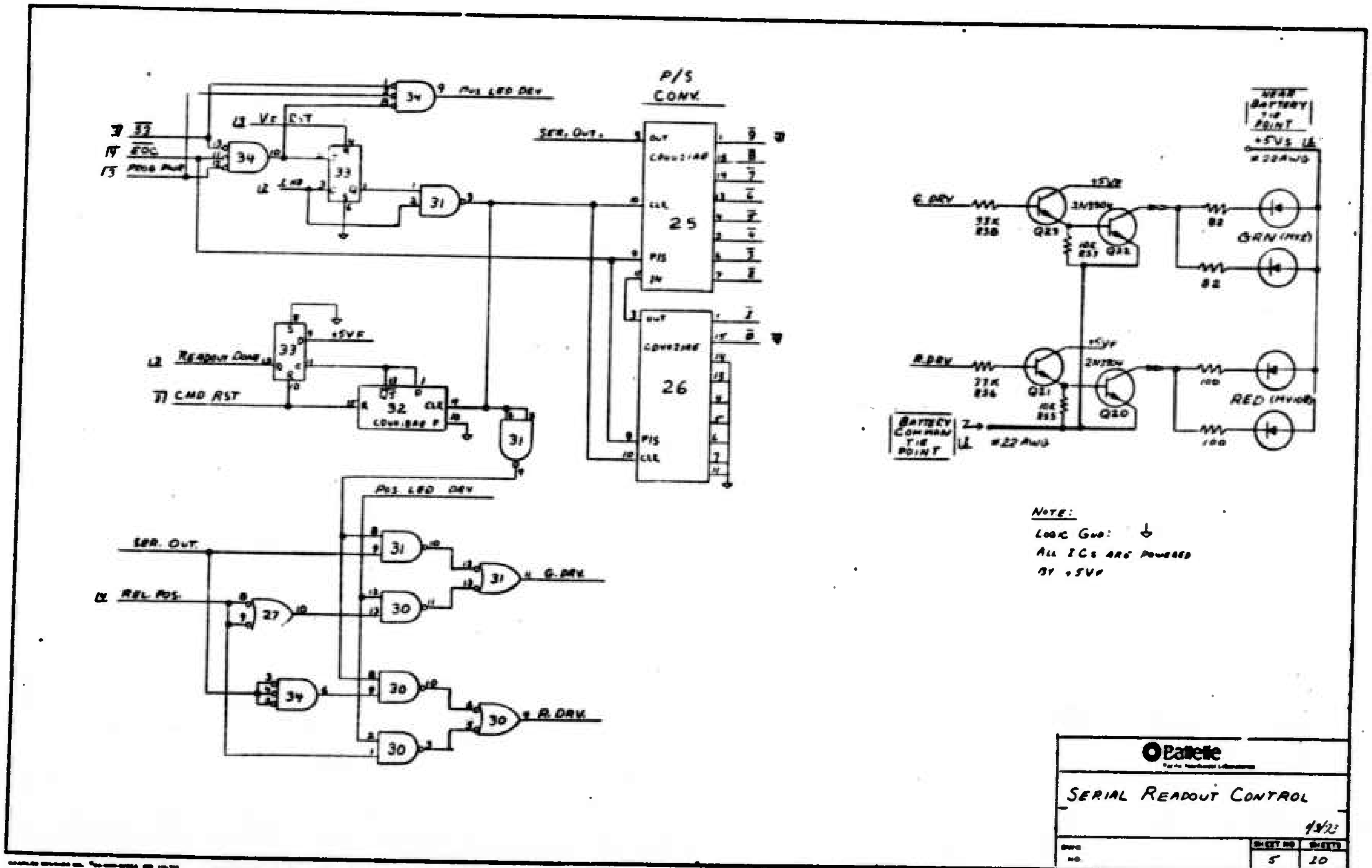


FIGURE A-5. Serial Readout Control

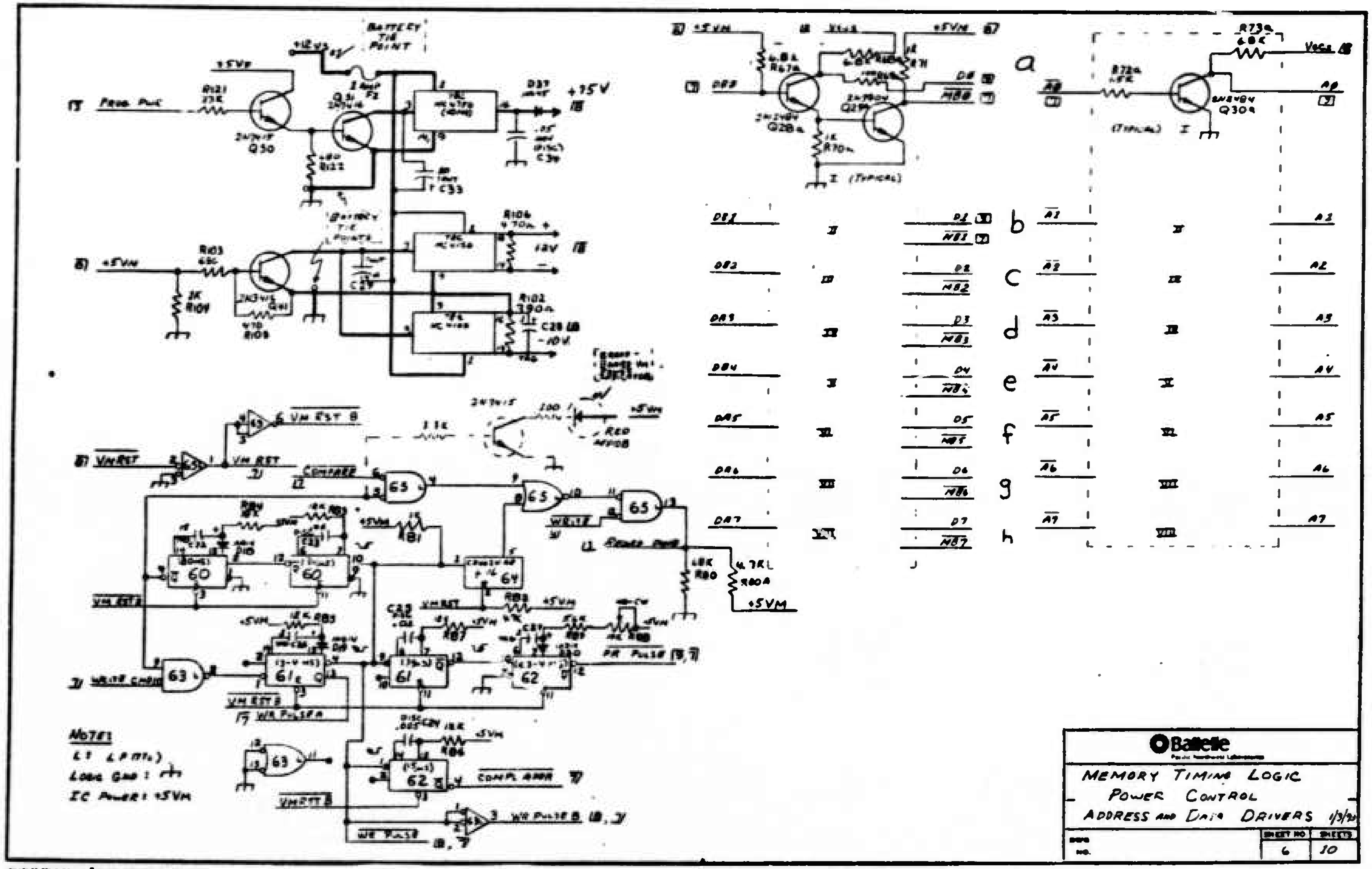


FIGURE A-6. Memory Timing Logic Power Control Address and Data Drivers

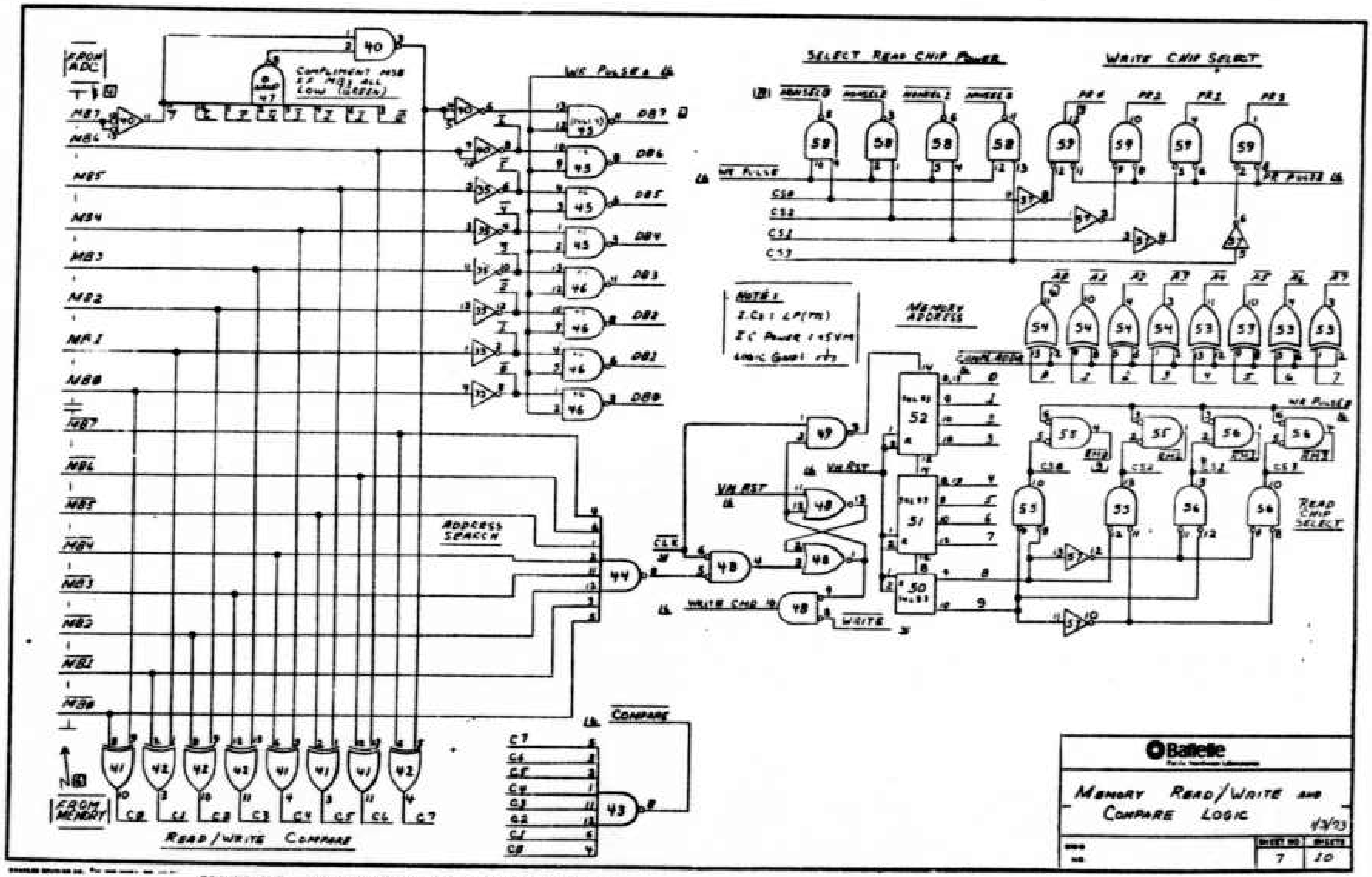


FIGURE A-7. Memory Read/Write and Compare Logic

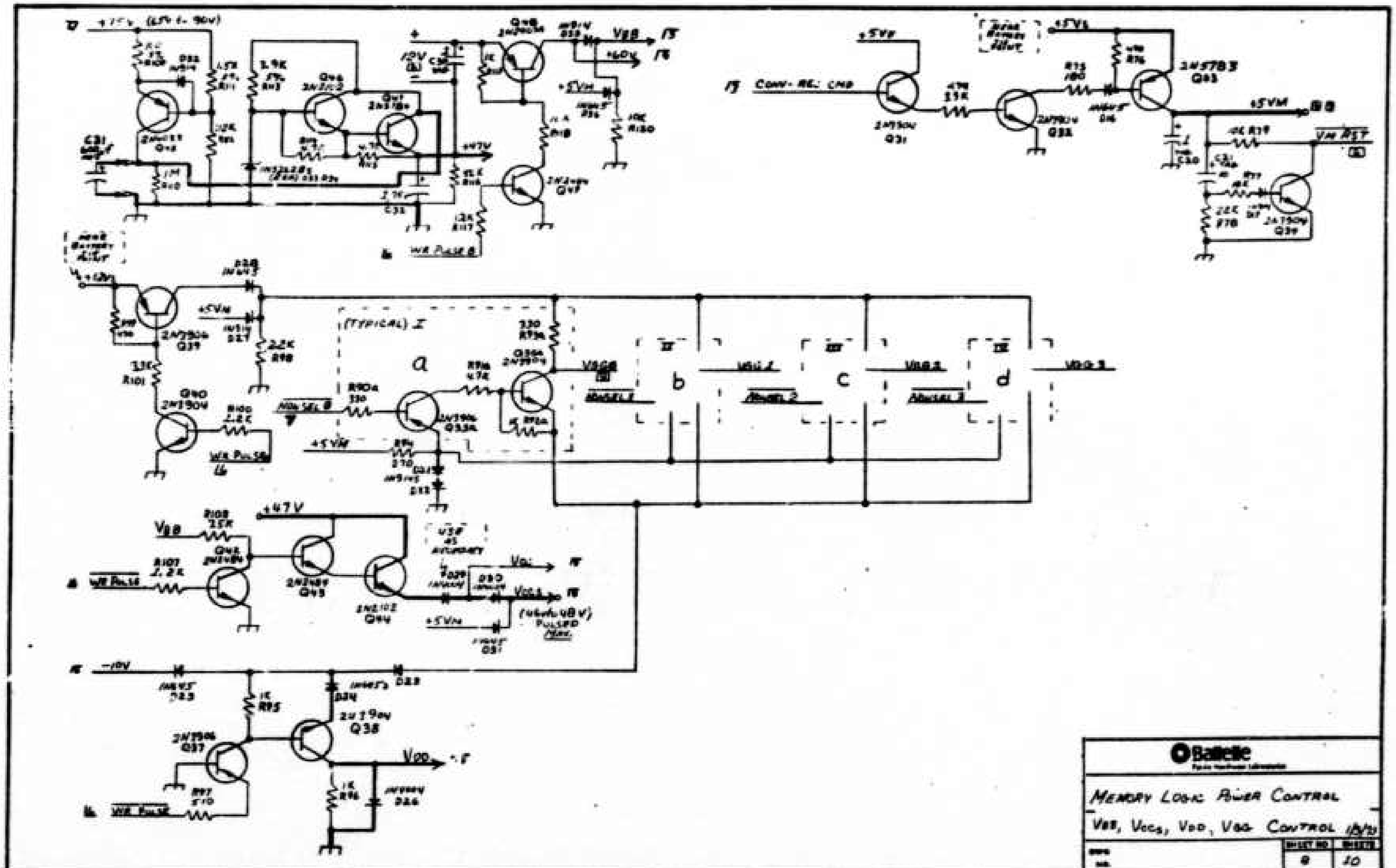


FIGURE A-8. Memory Logic Power Control
VBB, VCCS, VDD, VGG, Control

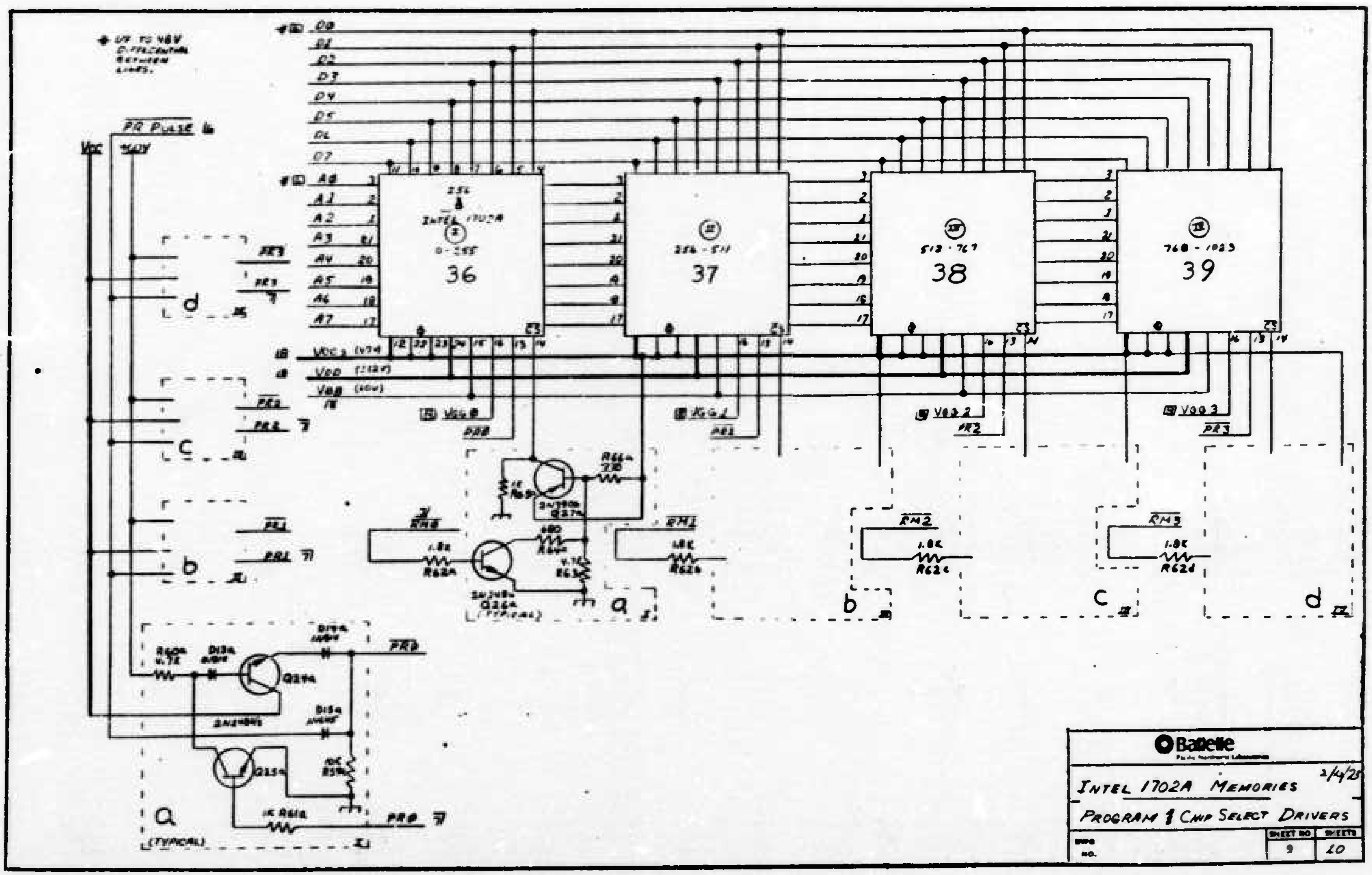


FIGURE A-9. Intel 1702A Memories Program and Chip Select Drivers

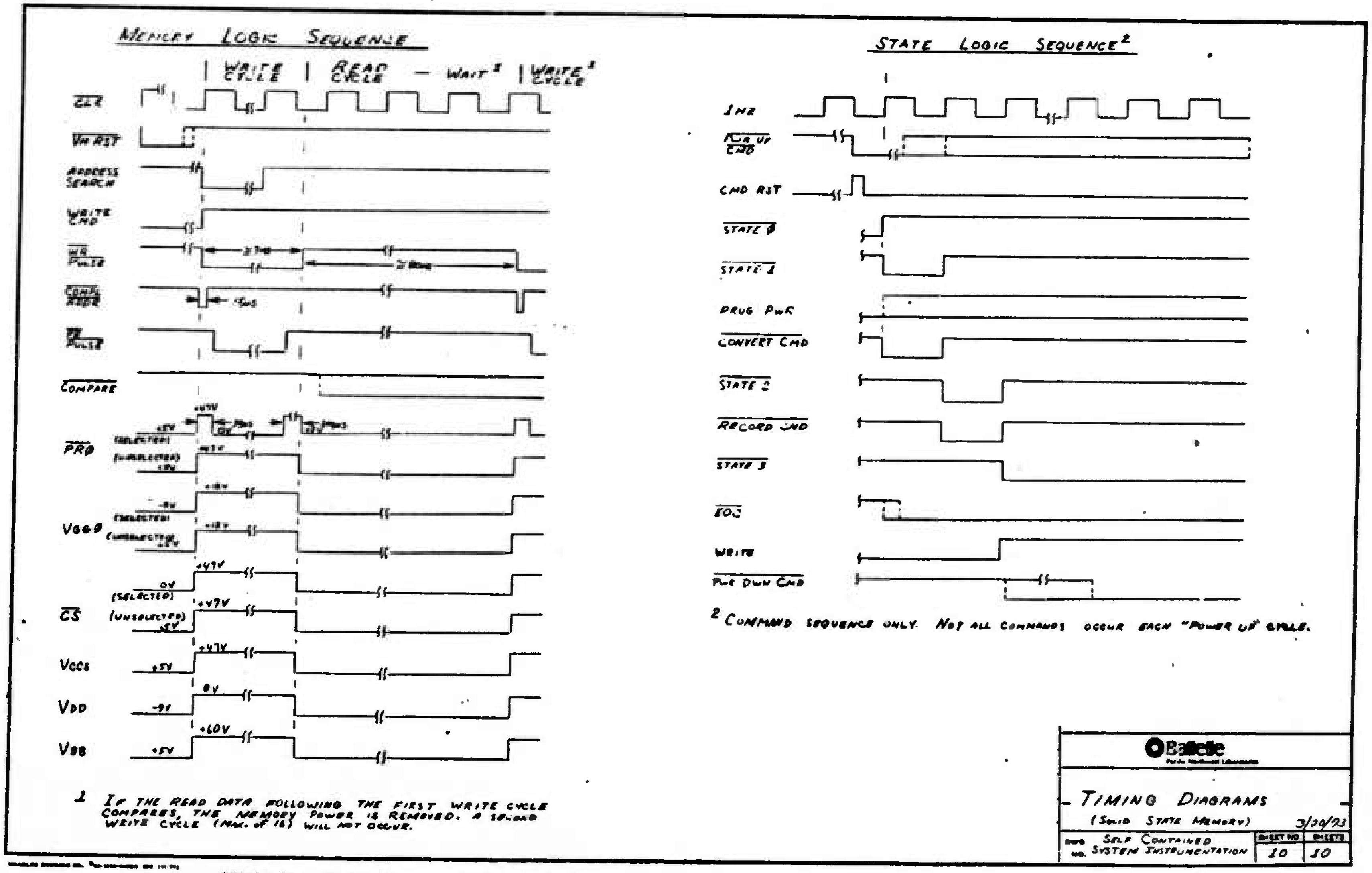


FIGURE 10. Timing Diagrams (Solid State Memory)

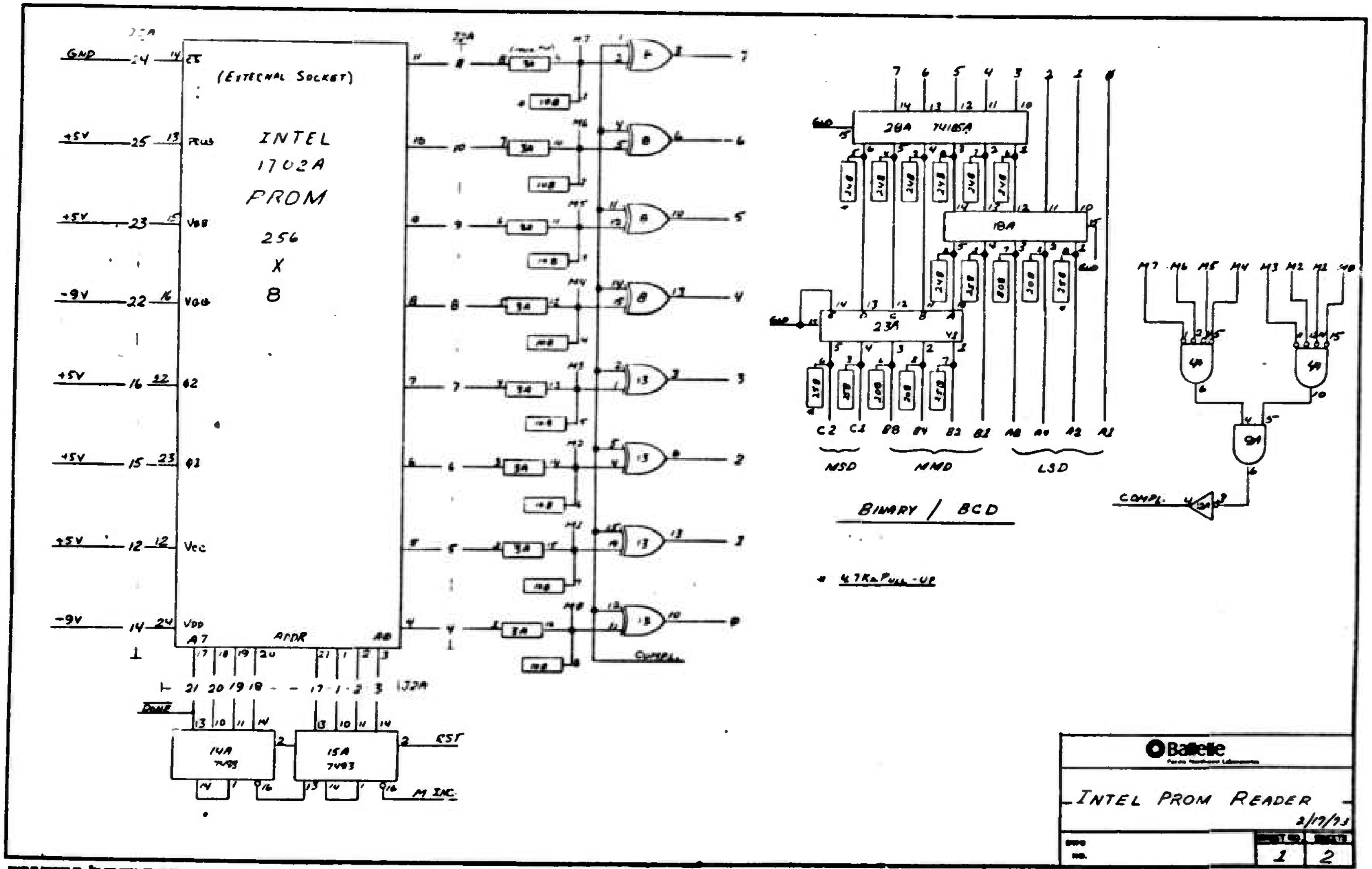


FIGURE A-11. Intel Prom Reader

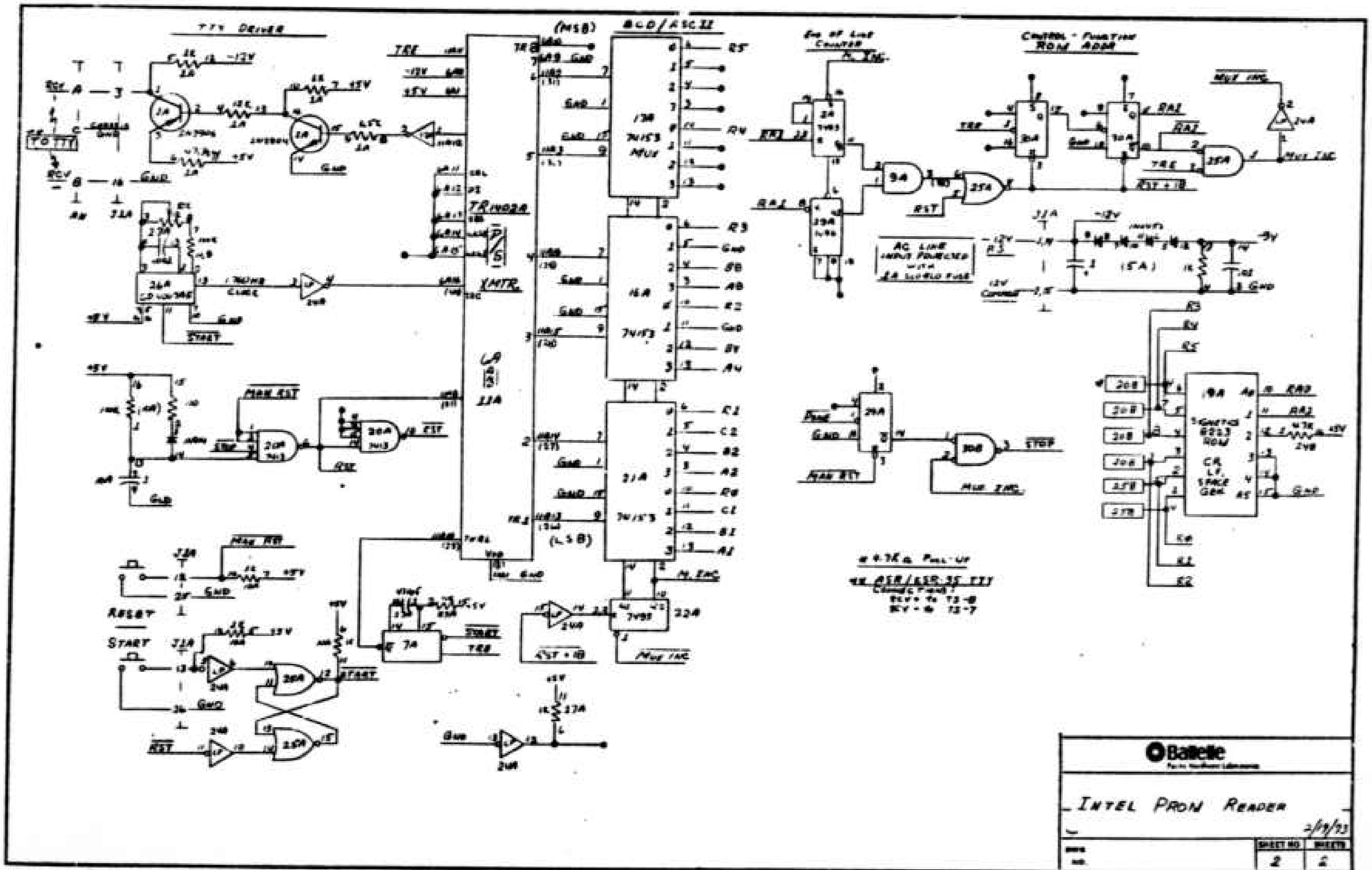
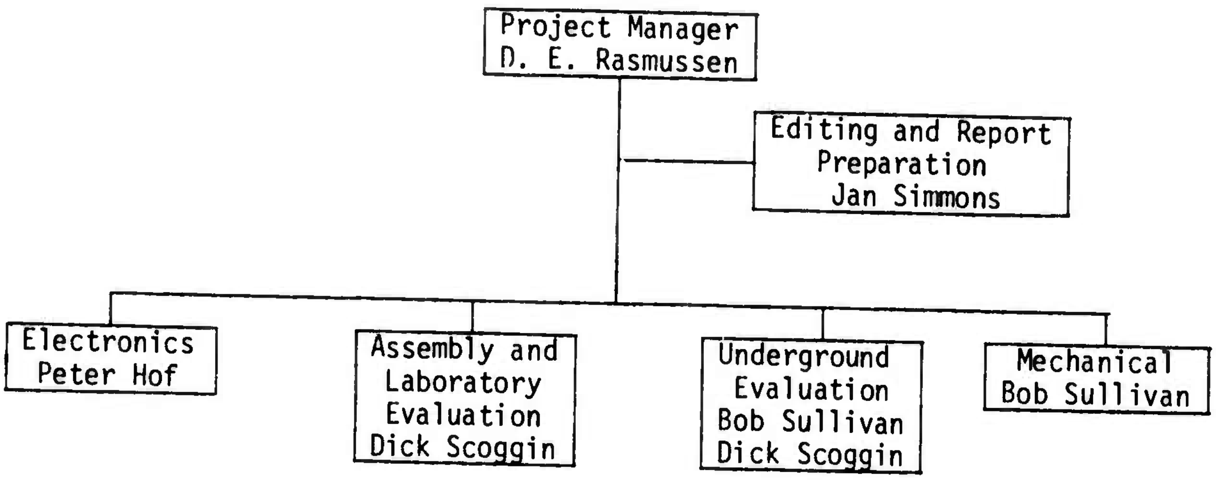


FIGURE A-12. Intel Prom Reader

ACKNOWLEDGMENTS

We would like to express our appreciation for the assistance we received from the U.S. Bureau of Mines, especially Mike Beus, in planning and arranging the instrument evaluation and demonstration work. Additionally, we appreciate the help provided by the Hecla Mining Company and their personnel at the Lucky Friday Mine, especially Gordon Pugh, for their help in the Prototype I underground evaluation. Without this kind of support, successful completion of the project would have been difficult.

Self-Contained System Project Organization



The following invention disclosures were transmitted to the sponsor under the subject contract:

OSIR-76 (MIN-1915) Compact and Self-Contained Rock Deformation Recorder
D. E. Rasmussen

OSIR-77 (MIN-1916) Miniature Punched Paper Tape Recorder
D. E. Rasmussen

OSIR-78 (MIN-1923) Magnetic Signal Connectors
J. T. Russell

OSIR-78 has been inactivated, and patent applications have not as yet been filed on the subject matter of OSIR-76 and -77.

Public Displays and Publications

- ARPA Review Meeting, Washington, D.C., February 16, 18, 1972
- AMC Coal Show, Cleveland, Ohio, May 8, 1972
- Spokane Mining Research Center Open House and U.S. Bureau of Mines Open Industry Briefing, April 10-12, 1973
- Spokane Mining Research Center Open House and Student Briefing, December 7, 1973.
- P. J. Hof, State-of-the-Art Probe Reports Underground Data, Instrumentation and Controls System Magazine, pp. 65-66, March 1974.